Terms used **richard york** Found **33** of **124,998**

Sort results by: relevance

Display results: expanded form

Save results to a Binder

Search Tips

Open results in a new window

Try an Advanced Search

Try this search in The ACM Guide

Results 1 - 20 of 33 Result page: **1** 2 next

Relevance scale

1 Transaction management I: Distributed database concurrency controls using before-values

Richard E. Stearns, Daniel J. Rosenkrantz

April 1981 **Proceedings of the 1981 ACM SIGMOD international conference on Management of data**

Full text available: pdf(1.08 MB) Additional Information: full citation, abstract, references, citings

Associated with the write of a database entity is both the "before" or old value, and the "after" or new value. Concurrency can be increased by allowing other transactions to read the before values of a given transaction. The ramifications of allowing this, particularly on a distributed system in which limited communications is desirable, are investigated. A careful distinction is made between design decisions concerning communications and design decisions concerning the responses to read/write ...

2 On the semantics of "now" in databases

James Clifford, Curtis Dyreson, Tomás Isakowitz, Christian S. Jensen, Richard T. Snodgrass

June 1997 **ACM Transactions on Database Systems (TODS)**, Volume 22 Issue 2

Full text available: pdf(819.31 KB) Additional Information: full citation, abstract, references, citings, index terms, review

Although "now" is expressed in SQL and CURRENT_TIMESTAMP within queries, this value cannot be stored in the database. How ever, this notion of an ever-increasing current-time value has been reflected in some temporal data models by inclusion of database-resident variables, such as "now" "until-changed, " "**," "@," and "-". Time variables are very desirable, but their u ...

Keywords: Now, SQL, TSQL2, indeterminacy, now-relative value, temporal query languge

3 Strongly-local reductions and the complexity/efficient approximability of algebra and optimization on abstract algebraic structures

Harry B. Hunt, Madhav V. Marathe, Richard E. Stearns

July 2001 **Proceedings of the 2001 international symposium on Symbolic and algebraic computation**

Full text available: pdf(816.66 KB) Additional Information: full citation, abstract, references, index terms

We demonstrate how the concepts of *algebraic representability* and *strongly-local reductions* developed here and in [20] can be used to characterize the computational

h be c g e cf

complexity/efficient approximability of a number of basic problems and their variants, on various abstract algebraic structures F. These problems include the following:

- Algebra: Determine the solvability, unique solvability, number of solutions, etc., of a system of equations on F. Determine the equival ...

4 An environment for research in microprogramming and emulation

Robert F. Rosin, Gideon Frieder, Richard H. Eckhouse

August 1972 **Communications of the ACM**, Volume 15 Issue 8

Full text available: pdf(1.33 MB) Additional Information: full citation, abstract, references, citings

The development of the research project in microprogramming and emulation at State University of New York at Buffalo consisted of three phases: the evaluation of various possible machines to support this research; the decision to purchase one such machine, which appears to be superior to the others considered; and the organization and definition of goals for each group in the project. Each of these phases is reported, with emphasis placed on the early results achieved in this research.

Keywords: computer systems, emulation, hardware evaluation, input-output systems, language processors, microprogramming, nanoprogram, project management

5 Session 9B: Pricing network edges for heterogeneous selfish users

Richard Cole, Yevgeniy Dodis, Tim Roughgarden

June 2003 **Proceedings of the thirty-fifth ACM symposium on Theory of computing**

Full text available: pdf(286.52 KB) Additional Information: full citation, abstract, references, citings, index terms

We study the negative consequences of selfish behavior in a congested network and economic means of influencing such behavior. We consider a model of selfish routing in which the latency experienced by network traffic on an edge of the network is a function of the edge congestion, and network users are assumed to selfishly route traffic on minimum-latency paths. The quality of a routing of traffic is measured by the sum of travel times (the *total latency*).It is well known that the outcome ...

Keywords: Nash equilibria, game theory, network pricing, selfish routing

6 How much can taxes help selfish routing?

Richard Cole, Yevgeniy Dodis, Tim Roughgarden

June 2003 **Proceedings of the 4th ACM conference on Electronic commerce**

Full text available: pdf(274.41 KB) Additional Information: full citation, abstract, references, citings, index terms

We study economic incentives for influencing selfish behavior in networks. We consider a model of selfish routing in which the latency experienced by network traffic on an edge of the network is a function of the edge congestion, and network users are assumed to selfishly route traffic on minimum-latency paths. The quality of a routing of traffic is historically measured by the sum of all travel times, also called the total latency.It is well known that the outcome of selfish routing (a Nash equ ...

Keywords: Nash equilibria, game theory, network pricing, selfish routing

7 Optimal VLSI circuits for sorting

Richard Cole, Alan Siegel

h be c g e cf

October 1988 **Journal of the ACM (JACM)**, Volume 35 Issue 4

Full text available: pdf(2.81 MB) Additional Information: full citation, abstract, references, citings, index terms

This work describes a large number of constructions for sorting N integers in the range [0, M - 1], for N ⩽ M ⩽ N2, for the standard VLSI bit model. Among other results, we attain: VLSI sorter constructions that are within a constant factor of optimal size, for all M and almost all running times T. a ...

8 Contributed articles: Dyadic execute

Richard H. Oates

March 1984 **ACM SIGAPL APL Quote Quad**, Volume 14 Issue 3

Full text available: pdf(1.02 MB) Additional Information: full citation, abstract, references

The quotes that distinguish a constant from a name are inconvenient in an expression dominated by constants, and they critically overload the quote character if monadic Execute is also used. When constants predominate, the declarative burden can be shifted to the names by means of a dyadic Execute function that takes a list of "names" as its left argument. A token in the right argument that does not appear in the left argument is a constant even when not enclosed in quotes. This technique would ...

9 Extending the message flow debugger for MQSI

Shuxia Tan, Eshrat Arjomandi, Richard Paige, Evan Mamas, Simon Moser, Bill O'Farrell

November 2001 **Proceedings of the 2001 conference of the Centre for Advanced Studies on Collaborative research**

Full text available: pdf(312.67 KB) Additional Information: full citation, abstract, references, index terms

Integration and management of applications play a key role in today's computing. MQSeries is an asynchronous, assured application-to-application communication protocol designed to support the integration of business processes. MQSeries Integrator (MQSI) is a component of MQSeries providing support for application integration and communication. The key technology in MQSI is the notion of a message flow. A message flow is a sequence of operations on a message, performed by a series of message proc ...

10 Interest made simple with arrays

Richard L. W. Brown

June 2000 **Proceedings of the international conference on APL-Berlin-2000 conference**, Volume 30 , 31 Issue 4 , 3

Full text available: pdf(448.84 KB) Additional Information: full citation, abstract, references, index terms

*A better financial calculator*Students of the mathematics of finance seem to be comfortable using calculators to evaluate formulas or numerical expressions. They are typically much less comfortable writing programs in BASIC (or C or Java etc.) even in situations where the calculator solution is tedious and a short program would do the job efficiently. Spreadsheet models, with an emphasis on formulas as opposed to programs, are quite a reasonable and intuitive tool. But spreadsheet formulas ...

11 Turing Award lecture: it's time to reconsider time

Richard Edwin Stearns

November 1994 **Communications of the ACM**, Volume 37 Issue 11

Full text available: pdf(3.16 MB) Additional Information: full citation, references, citings, index terms, review

12 Music: Approximate matching algorithms for music information retrieval using vocal input

h be c g e cf

Richard L. Kline, Ephraim P. Glinert
November 2003 **Proceedings of the eleventh ACM international conference on Multimedia**
Full text available: pdf(165.02 KB) Additional Information: full citation, abstract, references, index terms

Effective use of multimedia collections requires efficient and intuitive methods of searching and browsing. This work considers databases which store music and explores how these may best be searched by providing input queries in some musical form. For the average person, humming several notes of the desired melody is the most straightforward method for providing this input, but such input is very likely to contain several errors. Previously proposed implementations of so-called *query-by-humm ...*

Keywords: *music information retrieval, query by humming*

13 Virtual extension: Data warehousing in environmental digital libraries
Richard D. Holowczak, Nabil R. Adam, Francisco J. Artigas, Irfan Bora
September 2003 **Communications of the ACM**, Volume 46 Issue 9
Full text available: pdf(185.95 KB) Additional Information: full citation, references, index terms

14 Slowing down sorting networks to obtain faster sorting algorithms
Richard Cole
January 1987 **Journal of the ACM (JACM)**, Volume 34 Issue 1
Full text available: pdf(788.72 KB) Additional Information: full citation, abstract, references, citings, index terms, review

Megiddo introduced a technique for using a parallel algorithm for one problem to construct an efficient serial algorithm for a second problem. This paper provides a general method that trims a factor of O(log n) time (or more) for many applications of this technique.

15 Constrained nonlinear least squares: an exact penalty approach with projected structured quasi-Newton updates
Nezam Mahdavi-Amiri, Richard H. Bartels
September 1989 **ACM Transactions on Mathematical Software (TOMS)**, Volume 15 Issue 3
Full text available: pdf(1.49 MB) Additional Information: full citation, abstract, references, index terms, review

This paper is concerned with the development, numerical implementation, and testing of an algorithm for solving constrained nonlinear least squares problems. The algorithm is an adaptation of the least squares case of an exact penalty method for solving nonlinearly constrained optimization problems due to Coleman and Conn. It also uses the ideas of Nocedal and Overton for handling quasi-Newton updates of projected Hessians, those of Dennis, Gay, and Welsch for approaching the structure of n ...

16 Deterministic versus nondeterministic time and lower bound problems
Richard E. Stearns
January 2003 **Journal of the ACM (JACM)**, Volume 50 Issue 1
Full text available: pdf(36.62 KB) Additional Information: full citation, abstract, references, index terms

Because many problems of general interest have natural nondeterministic algorithms and because computers act deterministically, it is important to understand the relationship between deterministic and nondeterministic time. Specifically, it is important to understand how quickly a deterministic computing device can determine the outcome of a nondeterministic calculation. So far, we have no general techniques that work any better

than trying all step-by-step simulations, an exponential method.The ...

Keywords: Computational complexity, NP-completeness, SAT, generic algorithms, generic problems, nondeterminism, power index, time complexity

17 Contributed articles: Iota flow with direct local functions
Richard H. Oates
March 1981 **ACM SIGAPL APL Quote Quad**, Volume 11 Issue 3
Full text available: pdf(908.31 KB) Additional Information: full citation, references, citings

18 Column: Roots of equations
Richard N. Schmidt
July 1976 **ACM SIGAPL APL Quote Quad**, Volume 7 Issue 1
Full text available: pdf(403.40 KB) Additional Information: full citation

19 Applications: Customized geospatial workflows for e-government services
Richard D. Holowczak, Soon Ae Chun, Francisco J. Artigas, Vijayalakshmi Atluri
November 2001 **Proceedings of the ninth ACM international symposium on Advances in geographic information systems**
Full text available: pdf(1.80 MB) Additional Information: full citation, abstract, references

The past decade has experienced a phenomenal growth in the electronic delivery of business services. This has led to an elevation in the expectations of citizens for fast and efficient delivery of governmental services. Recently, workflow systems have gained importance as an effective= infrastructure for automating the business processes within and across government agencies. Government services, such as permit processing for the development or preservation of land, can be modeled as workflow. T ...

Keywords: customization, decision support, e-government services, geospatial workflow

20 Microprogrammed versus hardwired control units: how computers really work
Richard R. Eckert
September 1988 **ACM SIGCSE Bulletin**, Volume 20 Issue 3
Additional Information: full citation, index terms

Results 1 - 20 of 33 Result page: **1** 2 next

h be c g e cf

Terms used **real time debug for system on chip devices** Found **20** of **124,998**

Sort results by: relevance

Display results: expanded form

Save results to a Binder

Search Tips

Open results in a new window

Try an Advanced Search

Try this search in The ACM Guide

Results 1 - 20 of 20

Relevance scale

1 Support for real time and OS services in embedded systems: Synthesizing operating system based device drivers in embedded systems

Shaojie Wang, Sharad Malik

October 2003 **Proceedings of the 1st IEEE/ACM/IFIP international conference on Hardware/software codesign & system synthesis**

Full text available: pdf(205.33 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a correct-by-construction synthesis method for generating operating system based device drivers from a formally specified device behavior model. Existing driver development is largely manual using an ad-hoc design methodology. Consequently, this task is error prone and becomes a bottleneck in embedded system design methodology.Our solution to this problem starts by accurately specifying device access behavior with a formal model, viz. extended event driven finite state machin ...

Keywords: correct-by-construction, device driver, embedded system software, operating system based software synthesis

2 Session 8D: embedded tutorial: Test of future system-on-chips

Yervant Zorian, Sujit Dey, Michael J. Rodgers

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(140.88 KB) Additional Information: full citation, abstract, references

Spurred by technology leading to the availability of millions of gates per chip, system-level integration is evolving as a new paradigm, allowing entire systems to be built on a single chip. Being able to rapidly develop, manufacture, test, debug and verify complex SOCs is crucial for the continued success of the electronics industry. This growth is expected to continue full force at least for the next decade, while making possible the production of multimillion transistor chips. However, to mak ...

3 Analysis of hardware and software approaches to embedded in-circuit emulation of microprocessors

Hsin-Ming Chen, Chung-Fu Kao, Ing-Jer Huang

January 2002 **Australian Computer Science Communications , Proceedings of the seventh Asia-Pacific conference on Computer systems architecture - Volume 6**, Volume 24 Issue 3

Full text available: pdf(665.32 KB) Additional Information: full citation, abstract, references, index terms

h be c g e cf

This paper investigates various approaches to embed the functionality of in-circuit emulation (ICE) into microprocessor cores in SoC (System-On-Chip) chips. Three styles of ICE's (hardware-oriented, software-oriented and hybrid) are defined and implemented. They are integrated with a synthesizable ARM7 microprocessor core and synthesized to gate level to quantitatively analyze and compare their performance, cost and debugging features.

4 Low-power systems on chips (SOCs)
C. Piguet, M. Renaudin, T. Omnés
March 2001 **Proceedings of the conference on Design, automation and test in Europe**
Full text available: pdf(93.75 KB) Additional Information: full citation, references

5 Functional debugging of systems-on-chip
Darko Kirovski, Miodrag Potkonjak, Lisa M. Guerra
November 1998 **Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(548.22 KB) Additional Information: full citation, references, index terms

6 How application/technology evolutions will shape classical EDA?: System-on-chip beyond the nanometer wall
Philippe Magarshack, Pierre G. Paulin
June 2003 **Proceedings of the 40th conference on Design automation**
Full text available: pdf(454.87 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we analyze the emerging trends in the design of complex Systems-on-a-Chip for nanometer-scale semiconductor technologies and their impact on design automation requirements, from the perspective of a broad range SoC supplier.We present our vision of some of the key changes that will emerge in the next five years. This vision is characterized by two major paradigm changes. The first is that SoC design will become divided into four mostly non-overlapping distinct abstraction levels. ...

Keywords: design automation tools, embedded software technologies, multi-processor systems, network-on-chip, reconfigurable systems, system-on-chip

7 How Do You Design a 10M Gate ASIC?: Going mobile: the next horizon for multi-million gate designs in the semi-conductor industry
Christian Berthet
June 2002 **Proceedings of the 39th conference on Design automation**
Full text available: pdf(145.55 KB) Additional Information: full citation, abstract, references, index terms

The complexity of a System-on-Chip design is not only in the million transistors packed in a square millimeter. The major challenge for technical success of a SoC is to make sure that millions lines of software fit in with millions gates. In this paper, the problematic of multi-million gate design is illustrated from the viewpoint of a practical development of a complex digital system done at STMicroelectronics for a GSM/GPRS cellular application.

Keywords: HW/SW co-design, SoC design

8 Fast prototyping: a system design flow applied to a complex system-on-chip multiprocessor design

h be c g e cf

Benoit Clement, Richard Hersemeule, Etienne Lantreibecq, Bernard Ramanadin, Pierre Coulomb, Francois Pogodalla
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation conference**
Full text available: pdf(78.99 KB) Additional Information: full citation, references, citings, index terms

Keywords: fast prototyping, hardware/software (HW/SW) co-design, system design, system modeling, system verification, virtual component (VC) re-use

9 Special session on on-chip multi-processing: Design experience of a chip multiprocessor merlot and expectation to functional verification
Satoshi Matsushita
October 2002 **Proceedings of the 15th international symposium on System Synthesis**
Full text available: pdf(797.44 KB) Additional Information: full citation, abstract, references, index terms

We have fabricated a Chip Multiprocessor prototype code-named Merlot to proof our novel speculative multithreading architecture. On Merlot, multiple threads provide wider issue window beyond ordinal instruction level parallel (ILP) processors like superscalar or VLIW. With the architecture, we estimate 3.0 times speedup against single processing elements (PE) on speech recognition code and IDCT code with four PEs. Merlot integrates on-chip devices, PCI interface, and SDRAM interfaces. We have en ...

Keywords: CMP, chip multiprocessor, deign experience, functional verification, speculative multithreading

10 Challenges in the Design of a Scalable Data-Acquisition and Processing System-on-Silicon
January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**
Full text available: pdf(155.29 KB) Publisher Site Additional Information: full citation, abstract

Increasing complexity of the functionalities and the resultant growth in number of gates integrated in a chip coupled with shrinking geometries and short cycle time requirements bring in several challenges into the design of present day VLSI chips. In this paper we present the challenges faced and the approaches successfully adopted in the design of a complex 2.5 million gate high bandwidth data acquisition and processing VLSI chip (a trace-receiver chip, code-named Drishti) in a deep sub-micron ...

11 Built-in self-test for signal integrity
Mehrdad Nourani, Amir Attarha
June 2001 **Proceedings of the 38th conference on Design automation**
Full text available: pdf(149.79 KB) Additional Information: full citation, abstract, references, index terms

Unacceptable loss of signal integrity may harm the functionality of SoCs permanently or intermittently. We propose a systematic approach to model and test signal integrity in deep-submicron high-speed interconnects. Various signal integrity problems occurring on such interconnects (e.g. crosstalk, overshoot, noise, skew, etc.) are considered in a unified model. We also present a test methodology that uses a noise detection circuitry to detect low integrity signals and an inexpensive test ar ...

12 System level modeling and verification: Embedded systems verification with FGPA-

enhanced in-circuit emulator
M. Meerwein, C. Baumgartner, T. Wieja, W. Glauert
September 2000 **Proceedings of the 13th international symposium on System synthesis**

Full text available: pdf(109.43 KB) Additional Information: full citation, abstract, references, citings

In this paper we present a novel coverification concept for embedded microcontrollers that satisfies industrial requirements. Based on a commercially available CPU in-circuit emulator coupled with FPGA boards, it verifies the correctness of an implementation in terms of function and timing within a real-world environment.Using our system, the software engineer can write, test and optimize programs for a chip that is not yet physically existent. In addition the system is used to obtain software m ...

13 Development of processors and communication networks for embedded systems: Component-based design approach for multicore SoCs
W. Cesário, A. Baghdadi, L. Gauthier, D. Lyonnard, G. Nicolescu, Y. Paviot, S. Yoo, A. A. Jerraya, M. Diaz-Nava
June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(187.82 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents a high-level component-based methodology and design environment for application-specific multicore SoC architectures. Component-based design provides primitives to build complex architectures from basic components. This bottom-up approach allows design-architects to explore efficient custom solutions with best performances. This paper presents a high-level component-based methodology and design environment for application-specific multicore SoC architectures. The system speci ...

Keywords: HW/SW interfaces abstraction, component-based design, multicore System-on-Chip

14 System chip test: how will it impact your design?
Yervant Zorian, Erik Jan Marinissen
June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(107.58 KB) Additional Information: full citation, abstract, references, citings, index terms

A major challenge in realizing core-based system chips is the adoption and design-in of adequate test and diagnosis strategies. This tutorial paper discusses the specific challenges that come with testing deeply embedded reusable cores supplied by diverse providers, who often use different hardware description levels and mixed technologies. The paper describes a general test access architecture for embedded cores, and covers the current standardization efforts in this domain. In add ...

15 Focus on embedded systems
Rick Lehrbaum
June 2002 **Linux Journal**, Volume 2002 Issue 98

Full text available: html(15.50 KB) Additional Information: full citation, abstract, index terms

Embedded Systems Conference 2002

16 Keynote speech 4: Low power RF IC design for wireless communication
Domine M.W. Leenaerts
August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design**

Full text available: pdf(1.01 MB) Additional Information: full citation, abstract, references, index terms

h be c g e cf

In this paper, the many issues around the system and circuit design of advanced RF front ends for wireless RF applications will be discussed. After a short discussion on technology related issues, design choices linked to the different circuit/system solutions will be discussed.

Keywords: LNA, PLL, RF, VCO, low power, technology, transceivers, wireless communication

17 Re-configurable computing in wireless

Bill Salefski, Levent Caglar

June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(240.76 KB) Additional Information: full citation, abstract, references, citings, index terms

Wireless communications requires a new approach to implement the algorithms for new standards. The computational demands of these standards are outstripping the ability of traditional signal processors, and standards are changing too quickly for traditional hardware implementation. In this paper we outline how reconfigurable processing can meet the needs for wireless base station design while providing the programmability to allow not just field upgrades as standards evolve, but also to a ...

18 ICEBERG: an embedded in-circuit emulator synthesizer for microcontrollers

Ing-Jer Huang, Tai-An Lu

June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation conference**

Full text available: pdf(705.18 KB) Additional Information: full citation, references, citings, index terms

19 Scalable and flexible cosimulation of SoC designs with heterogeneous multi-processor target architectures

Patrice Gerin, Sungjoo Yoo, Gabriela Nicolescu, Ahmed A. Jerraya

January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation**

Full text available: pdf(214.44 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we present a cosimulation environment that provides modularity, scalability, and flexibility in cosimulation of SoC designs with heterogeneous multi-processor target architectures. Our cosimulation environment is based on an object-oriented simulation environment, SystemC. Exploiting the object orientation in SystemC representation, we achieve modularity and scalability of cosimulation by developing modular cosimulation interfaces. The object orientation also enables mixed-le ...

20 How to Choose Semiconductor IP: Embedded Software

G. Martin

March 2002 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(49.32 KB) Additional Information: full citation

Publisher Site

Results 1 - 20 of 20

h be c g e cf

Your search matched **4** of **989552** documents.

A maximum of **4** results are displayed, **15** to a page, sorted by **Relevance** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the text box.
Then click **Search Again**.

((real <and> time <and> debug) and ((1999 <in> py))) Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **Using the BS register for capturing and storing n-bit sequences in re**

Alves, G.R.; Ferreira, J.M.M.;
Test Workshop 1999. Proceedings. European , 25-28 May 1999
Page(s): 130 -135

[Abstract] [PDF Full-Text (292 KB)] **IEEE CNF**

2 **Testing semiconductor chips: trends and solutions**
Zorian, Y.;
Integrated Circuits and Systems Design, 1999. Proceedings. XII Symposium on
Sept.-2 Oct. 1999
Page(s): 226 -233

[Abstract] [PDF Full-Text (188 KB)] **IEEE CNF**

3 **An integrated approach for real-time system design**
Lichen Zhang; Peijiang Yuan;
Communications, Computers and Signal Processing, 1999 IEEE Pacific Rim Conf
on , 22-24 Aug. 1999
Page(s): 63 -66

[Abstract] [PDF Full-Text (400 KB)] **IEEE CNF**

4 **Automatic distribution of reactive systems for asynchronous networ**
processors
Caspi, P.; Girault, A.; Pilaud, D.;

h e ch eee e eee g e ch c e e ch e ch ge e

Software Engineering, IEEE Transactions on , Volume: 25 Issue: 3 , May-June
Page(s): 416 -427

[Abstract] [PDF Full-Text (404 KB)] **IEEE JNL**

h e ch eee e eee g e ch c e e ch e ch ge e

With respect to claim 4, Assouad et al disclose the subject matter discussed supra with respect to claim 1, upon which the instant claim depends.

The difference between the instant claim and Assouad et al is the explicit recitation that the cache memory is 512K bytes in size. Assouad et al do disclose a memory buffer of "sufficient size" in column 3, lines 41-42.

However, Kirk discloses a 512K byte data cache, which is implicitly "sufficient," in column 9, line 67.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of Assouad et al and Kirk before him/her, to utilize a 512K byte cache of Kirk in the system of Assouad et al because it is, "...of sufficient size to handle host requests," as discussed by Assouad et al in column 3, lines 40-44. Also, MPEP 2144.04 IV. A. recites:

"In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955) (Claims directed to a lumber package "of appreciable size and weight requiring handling by a lift truck" where held unpatentable over prior art lumber packages which could be lifted by hand because limitations relating to the size of the package were not sufficient to patentably distinguish over the prior art.); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976) ("mere scaling up of a prior art process capable of being scaled up, if such were the case, would not establish patentability in a claim to an old process so scaled." 531 F.2d at 1053, 189 USPQ at 148.)."

"In Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984), the Federal Circuit held that